**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Currently Amended) A phase-locked loop circuit for providing an output signal having a frequency depending on the frequency of a reference signal, the circuit comprising:

means for deriving a feedback signal from the output signal;

means for providing a control signal indicative of a phase difference between the reference signal and the feedback signal;

means for controlling the frequency of the output signal according to the control signal; and

means for conditioning the control signal through a conditioning signal, wherein

the means for conditioning includes means for accumulating energy provided by the control signal and the conditioning signal during a first phase and for transferring the accumulated energy to the means for controlling the frequency of the output signal during a second phase; and means for selectively applying the control signal and the conditioning signal to the energy accumulation means.

2. (Original) The circuit according to claim 1, wherein the means for conditioning includes capacitive means, first switching means responsive to a first enabling signal for coupling the capacitive means with the means for providing the control signal during the first phase, and second switching means responsive to a second enabling signal for coupling the capacitive means with the means for controlling the frequency of the output signal during the second phase.

3. (Original) The circuit according to claim 1, wherein the phase-locked loop circuit is of the fractional type for synthesizing the output signal multiplying the frequency of the reference signal by a fractional conversion factor, the means for deriving the feedback signal including means for dividing the frequency of the output signal by a dividing ratio being modulated to provide the conversion factor on the average, and wherein the means for conditioning includes means for providing a first conditioning signal for compensating a phase error caused by the modulation of the dividing ratio, the control signal consisting of a series of pulses modulated according to a first technique and the first conditioning signal consisting of a series of pulses modulated according to a second technique.

4. (Original) The circuit according to claim 3, further including means for providing a correction value indicative of the phase error, the correction value having at least one bit, and wherein the means for providing the first conditioning signal includes a digital-to-analog converter of a switched-capacitor type for converting the correction value into the first conditioning signal, the converter being controlled by the first and the second enabling signals.

5. (Original) The circuit according to claim 4, wherein the converter includes an output capacitor and, for each bit of the correction value, an input capacitor, a first switch for connecting the input capacitor to a power supply source in response to the second enabling signal and the corresponding bit, and a second switch for connecting the input capacitor to the output capacitor in response to the first enabling signal, the conditioning means including a further first switch for connecting the output capacitor to the means for providing the control signal in response to the first enabling signal and a further second switch for connecting the output capacitor to the means for controlling the frequency of the output signal in response to the second enabling signal.

6. (Original) The circuit according to claim 4, wherein the converter includes, for each bit of the correction value, an input capacitor, a first switch for connecting the input capacitor to a power supply source in response to the first enabling signal and the

corresponding bit, and a second switch for connecting the input capacitor to the means for controlling the frequency of the output signal in response to the second enabling signal, the conditioning means including a further capacitor, a further first switch for connecting the further capacitor to the means for providing the control signal in response to the first enabling signal, and a further second switch for connecting the further capacitor to the means for controlling the frequency of the output signal in response to the second enabling signal.

7. (Original) The circuit according to claim 4, wherein the correction value includes a plurality of bits, the converter further including means for converting the bits of the correction value into a plurality of thermometric bits of even weight.

8. (Original) The circuit according to claim 7, wherein the converter further includes means for scrambling the thermometric bits.

9. (Original) The circuit according to claim 1, wherein the means for conditioning includes means for providing a second conditioning signal for causing the circuit to enter a lock condition when the reference signal and the feedback signal have the same frequency and a pre-defined phase difference, the control signal consisting of a series of pulses and the second conditioning signal having a constant amplitude corresponding to the pre-defined phase difference.

10. (Currently Amended) In a fractional-type phase-locked loop circuit, a method of providing an output signal having a frequency depending on the frequency of a reference signal, the method comprising the steps of:

deriving a feedback signal from the output signal;

providing a control signal indicative of a phase difference between the reference signal and the feedback signal;

controlling the frequency of the output signal according to the control signal; and

conditioning the control signal through a conditioning signal, wherein

accumulating energy provided by the control signal and the conditioning signal ~~during~~ responsive to a first phase of the reference signal, and

transferring the accumulated energy for controlling the frequency of the output signal ~~during~~ responsive to a second phase of the reference signal.

11. (Original) A phase-locked loop circuit for providing an output signal having a frequency depending on the frequency of a reference signal, the circuit comprising:

a charge pump generator including an output terminal;

a signal filter; and

a first compensation circuit connected to an intermediate node between the output terminal of the charge pump generator and the signal filter, the first compensation circuit including:

a plurality of energy storage legs connected to the intermediate node and controlled by respective bits of a digital compensation signal, each energy storage leg being structured to store charge during a first phase if the bit controlling the energy storage leg is active and output the stored charge during a second phase.

12. (Original) The circuit of claim 11, wherein the first compensation circuit further includes a first capacitor connected between the energy storage legs and the intermediate node.

13. (Original) The circuit of claim 12, wherein the first compensation circuit further includes an amplifier connected between the energy storage legs and the intermediate node, the first capacitor being connected between an input and an output of the amplifier.

~~15~~14. (Currently Amended) The circuit of claim 12 wherein the first compensation circuit further includes a first switch connected between the output of the charge pump and a first plate of the first capacitor and a second switch connected between the first plate

of the first capacitor and the signal filter, the first and second switches being driven in phase opposition.

~~16~~15. (Currently Amended) The circuit of claim ~~15~~ 14 wherein each energy storage leg includes a second capacitor, a third switch connected between the second capacitor and the first capacitor, and a fourth switch connected between the second capacitor and a voltage reference; the first and third switches being controlled by a first control signal to open and close in tandem, and the second and fourth switches being controlled by a second control signal to open and close in tandem and in opposition to the first and third switches.

~~17~~16. (Currently Amended) The circuit of claim 11 wherein each energy storage leg includes:

an energy storage element;

a switch connected between a voltage reference and the energy storage element; and

an AND gate having a first input receiving the respective bit of the digital compensation signal, a second input receiving a phase control signal, and an output connected to a control terminal of the switch.

~~18~~17. (Currently Amended) The circuit of claim 11, further including a second compensation circuit connected between the output of the charge pump and the signal filter, the second compensation circuit including a first energy storage element.

~~19~~18. (Currently Amended) The circuit of claim ~~18~~ 17 wherein the second compensation circuit further includes a first switch connected between the output of the charge pump and the first energy storage element and a second switch connected between the first energy storage element and the signal filter, the first and second switches being driven in phase opposition.

~~20~~19. (Currently Amended) The circuit of claim ~~19~~18 wherein each energy storage leg includes a second energy storage element, a third switch connected between the intermediate node and the second energy storage element, and a fourth switch connected between the second energy storage element and a voltage reference; the first and fourth switches being controlled by a first control signal to open and close in tandem, and the second and third switches being controlled by a second control signal to open and close in tandem and in opposition to the first and fourth switches.

20. (New) The circuit of claim 1 wherein the first phase is a first phase of a period of the reference signal and the second phase is a second phase of the period of the reference signal.

21. (New) The circuit of claim 20 wherein the first phase consists of a fist half-period of the reference signal and the second phase consists of a second half-period of the reference signal.

22. (New) The method of claim 10 wherein the accumulating step includes accumulating the energy in an energy storage element in response to a first phase of a period of the reference signal and the transferring step includes transferring the accumulated energy in response to a second phase of the period of the reference signal.

23. (New) A fractional phase-locked loop circuit for synthesizing an output signal having a frequency depending on a multiplication of a frequency of a reference signal by a fractional conversion factor, the circuit comprising:

means for deriving a feedback signal from the output signal that includes means for dividing the frequency of the output signal by a dividing ratio being modulated to provide the conversion factor on the average;

means for providing a control signal indicative of a phase difference between the reference signal and the feedback signal;

means for controlling the frequency of the output signal according to the control signal;

means for conditioning the control signal through a conditioning signal, wherein the means for conditioning includes:

means for accumulating energy provided by the control signal and the conditioning signal during a first phase and for transferring the accumulated energy to the means for controlling the frequency of the output signal during a second phase; and

means for providing a first conditioning signal for compensating a phase error caused by the modulation of the dividing ratio, the control signal consisting of a series of pulses modulated according to a first technique and the first conditioning signal consisting of a series of pulses modulated according to a second technique.

24. (New) The circuit according to claim 23, further including means for providing a correction value indicative of the phase error, the correction value having at least one bit, and wherein the means for providing the first conditioning signal includes a digital-to-analog converter of a switched-capacitor type for converting the correction value into the first conditioning signal, the converter being controlled by the first and the second enabling signals.

25. (New) The circuit according to claim 24, wherein the converter includes an output capacitor and, for each bit of the correction value, an input capacitor, a first switch for connecting the input capacitor to a power supply source in response to the second enabling signal and the corresponding bit, and a second switch for connecting the input capacitor to the output capacitor in response to the first enabling signal, the conditioning means including a further first switch for connecting the output capacitor to the means for providing the control signal in response to the first enabling signal and a further second switch for connecting the output capacitor to the means for controlling the frequency of the output signal in response to the second enabling signal.

26. (New) The circuit according to claim 24, wherein the converter includes, for each bit of the correction value, an input capacitor, a first switch for connecting the input capacitor to a power supply source in response to the first enabling signal and the corresponding bit, and a second switch for connecting the input capacitor to the means for controlling the frequency of the output signal in response to the second enabling signal, the conditioning means including a further capacitor, a further first switch for connecting the further capacitor to the means for providing the control signal in response to the first enabling signal, and a further second switch for connecting the further capacitor to the means for controlling the frequency of the output signal in response to the second enabling signal.

27. (New) The circuit according to claim 24, wherein the correction value includes a plurality of bits, the converter further including means for converting the bits of the correction value into a plurality of thermometric bits of even weight.

28. (New) The circuit according to claim 27, wherein the converter further includes means for scrambling the thermometric bits.